WHAT IS CLAIMED IS:

1. A method of programming a PMOS stacked gate memory cell that includes spaced apart p-type diffusion regions formed in an n-type semiconductor substrate to define a substrate channel region therebetween, a conductive floating gate electrode formed over the channel region and separated therefrom by gate dielectric material, and a conductive control gate electrode formed over the floating gate electrode and separated therefrom by intergate dielectric material, the method comprising:

a. applying a negative voltage bias to the drain region of the PMOS memory cell;

b. applying a voltage pulse to the control gate electrode of the PMOS memory cell such that electrons are attracted to the floating gate electrode through the gate dielectric material; and

c. repeating step b to provide a sequence of voltage pulses to the control gate electrode such that the floating gate electrode is brought to a selected potential that is negative, but lower in absolute value compared with the drain potential.